AVINASH KUMAR GUPTA
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ACADEMIC DETAILS

Education	University	Year	CGPA
Master's in Electrical and Computer Engineering	University of Michigan - Ann Arbor	2022 - Present	4/4
Bachelor of Technology in Electrical Engineering	Indian Institute of Technology, Ropar (IIT Ropar)	2016 - 2020	8.11/10

AREAS OF INTEREST

Analog Circuit Design, FETs & Memory Device Modeling & Crossbar Simulation, Neuromorphic Electronics

TECHNICAL SKILLS

Microcontrollers Used (Raspberry Pi, Arduino) **Languages** (MATLAB, VerilogA, C, Python, HTML, Javascript), **Operating System** Linux, Windows **VLSI Design** (Cadence Spectre & Virtuoso, LTSpice, Magic VLSI), FPGA Simulation (Using Vivado), COMSOL Multiphysics, TCAD Sentaurus, Ansys EDT (Buffer and SerDes Channel Simulation)

EXPERTISE

1. **Analog Circuit Design** – Operational Amplifier Design, Active Baseband Filter Design for 5G Bandwidth Modes, Buffer Modeling using IBIS.
2. **Undergraduate Research Focus** – Resistive random-access memory (RRAM) device modeling and Crossbar circuit simulation, 2D Transition Metal Dichalcogenides (TMDs)-based FETs modeling and simulation.
3. **JRA Research Focus (CUHK, Hong Kong SAR)** – Numerical modeling of a high-speed graphene-on-silicon nitride waveguide photodetector temporal response

ACADEMIC & PROFESSIONAL EXPERIENCE

1. **Graduate Research Assistant**
   (Dr. Mehdi Saligane, University of Michigan, USA, NIST & Google Sponsored Project) *(Feb'23 - Present)*
   - **Peripheral circuitry design for novel neuromorphic and memory devices characterisation and testing**
2. **Undergraduate Researcher**
   (Dr. Brajesh Rawat's Lab, IIT Ropar, INDIA) *(May'18 - Jun'20)*
   - **Metal-Oxide-based RRAM Device Modeling and Crossbar Memory Circuit Simulation**
   - **Two Dimensional Transition Metal Dichalcogenides-based FETs Modeling and Circuit Simulation**
3. **Analog Design Engineer**
   (Signalchip Innovations, Bangalore, INDIA) *(Jul'20 - Apr'21)*
   - **Operational Amplifier Design**
     - Designed an OTA and trickle bias circuit (65-nm technology node)
     - Worked on Layout– Design Rule Check and Layout Versus Schematic
     - Back annotated for performance degradation post layout
   - **Analog Tx and Rx Baseband Filter Design for 5G BW Modes**
     - Designed a 3^{rd} and 5^{th} order Chebyshev Active-RC low pass filter for Rx and Tx respectively
     - Implemented frequency characteristics using switched resistance and capacitance banks
     - Back annotated for performance degradation post layout
   - **IBIS Buffer Modeling**
     - Tailored an IBIS modeling toolkit for the company using S2IBIS open-source code
     - Developed industry standard buffer models for GPIO, DDR IO, differential SGMII/RGMII Tx/Rx buffers by creating netlist from the back annotated testbench
     - Assumed full responsibility to handle all the IBIS-related development and client requests
4. **Junior Research Assistant (Research Internship)**
   (Prof. Hon Ki Tsang's Lab, Chinese University of Hong Kong (CUHK), Hong Kong SAR) *(Jun'19 - Aug'19)*
   - **Modeling the contribution of carrier diffusion in high-speed graphene photodetectors** *(fully independent)*
     - **Objective**: To investigate and model the carrier diffusion in the graphene-on-Si_3N_4 photodetectors and match with the experimental transient response of the device.
     - Wrote MATLAB codes to apply three different models, namely the ambipolar transport model, the drift-diffusion model, and the band model, to study the carrier dynamics due to diffusion in the channel (μm-range)
     - Accommodated surface plasmon effect near the metal and graphene interface where carrier generation is high due to the enhancement of the EM-field
     - Imported I-V characteristics obtained from MATLAB simulation code to model photodetector using VerilogA
     - Simulated experimental circuit setup in Cadence Spectre with good accuracy match

RESEARCH & CONFERENCE PAPERS (Google Scholar Link)

1. **Avinash Kumar Gupta**, M. S. Yadav and Brajesh Rawat, "Device-Circuit Co-optimization of Niobium Oxide-based Memristor for Large-Scale Crossbar Memory," ***(Preprint TechRxiv)***.

2. Mani Shankar Yadav, **Avinash Kumar Gupta**, Kanupriya Varshney and Brajesh Rawat, "How Good Silicon Oxide-based Memristor Can be?," **35th IEEE International Conference on VLSI Design, Virtual**, 26 Feb-2 Mar, **2022** (Accepted: Regular Paper).

3. **Avinash Kumar Gupta** & M. S. Yadav, Brajesh Rawat, "Role of Resistive Layer in Threshold Memory Switching Memristor Device," **4th International Conference on Memristive Materials, Devices and Systems (MEMRISYS)**, **Tsukuba, Japan**, 1-4 Nov **2021** (Oral Presentation).

4. Akhilesh Rawat, **Avinash Kumar Gupta** and Brajesh Rawat, "Performance Projection of Two-dimensional Material based CMOS Inverters for Sub-10 nm Channel Length," ***IEEE Transactions on Electron Devices***, vol. 68, no. 7, pp. 3622-3629, July **2021**. (Cited by- 3, IF- 2.92)

5. Aditya Kuber Parit, Mani Shankar Yadav, **Avinash Kumar Gupta**, Brajesh Rawat, "Design and modeling of Niobium Oxide-Tantalum Oxide-based self-selective memristor for large-scale crossbar memory," ***Elsevier Chaos Solitons & Fractals Journal***, vol. 145, p. 110818, March **2021**. (Cited by- 12, IF- 9.92)

6. Akhilesh Rawat, **Avinash Kumar Gupta**, Brajesh Rawat, "High-Performance Single and Multilayer Black Phosphorous-based CMOS Inverter for Deep Sub-10-nm Technology," **20th International Workshop on Physics of Semiconductor Devices**, **Kolkata, India**, 17-20 Dec **2019**. (Poster Presentation)

RELEVANT RESEARCH PROJECTS

1. **Device-circuit Co-design of Self-Selective Memristor based on Niobium Oxide for Large-Scale Crossbar Array** *(fully independent)*
(Guide: Dr Brajesh Rawat, IIT Ropar, INDIA) ***(B.Tech Capstone Project)*** *(Jan'19 - Mar'21)*
   - **Objective**: To mitigate the sneak current for large-scale implementation of niobium oxide RRAM-based crossbar array
   - Simulated physics-based numerical device model for self-selective niobium-oxide memristor in COMSOL
   - Imported I-V characteristics of the device for crossbar circuit simulation in Cadence Spectre using Verilog-A
   - Proposed a modified crossbar array architecture to reduce the sneak current improving power and readout margind with smaller area coverage
   - Authored the submission of the work in *IEEE Transaction on Nanotechnology* journal (under review)

2. **Electro-thermal model of resistive switching in metal-oxide-based RRAM using COMSOL** *(fully independent)*
(Guide: Dr. Brajesh Rawat, IIT Ropar, INDIA) *(Aug'19 - Sep'20)*
   - **Objective**: To model the electro-thermal resistive switching in metal-oxide RRAM structure
   - Simulated physics-based numerical model for NbO_X ,HfO_X, and TaO_X RRAM structure in COMSOL
   - Compared variation of device metrics (V_{SET}, V_{RESET}, current, switching speed) with varying thermal conditions and geometry
   - Presented results at Memrisys Conference 2021, Japan

3. **Performance analysis of Transition Metal Dichalcogenide (TMD) Field-Effect Transistors**
(Guide: Dr. Brajesh Rawat, IIT Ropar, INDIA) *(May'18 - Jun'19)*
   - **Objective**: To investigate the performance of CMOS inverters based on MoS_2-, WS_2-, WSe_2-, WSe_2-MoS_2 and black phosphorus-based FETs in sub-10 nm regime
   - Collaborated with a research scholar for a developing quantum transport model of ultra-scaled devices
   - Implemented the drain current and terminal charges from Green's function to develop the device model in Verilog-A for circuit simulation
   - Performed static (gain and noise margin) and dynamic (delay, power, and power-delay product) performance analysis of inverter in Cadence Spectre
   - Co-authored the work in *IEEE Transaction on Electron Devices* journal

4. **2D materials based device modeling**
(Guide: Dr. Brajesh Rawat, IIT Ropar) *(May'18 - Dec'18)*
   - **Objective**: To model graphene nanoribbon (GNR), bilayer graphene (BLG), and bilayer graphene (BLGNR) FETs
   - Wrote a MATLAB code for solving non-equilibrium green's function (NEGF)
   - Modified Hamiltonian matrix for varying channel materials to incorporate the changes in material properties

RELEVANT ACADEMIC PROJECTS

1. **Design of an Automated Gain Control (AGC) Amplifier**
(Guide: Dr Ehsan Afshari, University of Michigan, August'22 - Dec'22) ***(Course Project)***
   - Designed and simulated an AGC architecture in Cadence Virtuoso based on 130 nm CMOS process technology for a wireless receiver chain
   - Implemented the AGC based on a feedback architecture with an input dynamic range of 0.3 μV to 300 μV (60 dB)

2. **An attendance and digital entrance record system for library and college entry using Face recognition and a smart lock that unlocks by detecting the faces**
(Guide: Dr Rohit Y. Sharma, IIT Ropar, INDIA) *(Aug'17 - Nov'17)*
    - In a group of 2 students, designed a face recognition system for recording the entry and exit time of students and visitors
    - Implemented digital attendance of the students in a lecture hall and email the attendance record to Professor
    - Used the Haar cascades for the face detection and recognition using OpenCV and python on the Raspberry Pi and Pi-cam
    - Deployed IR sensor to count the number of students entering and comparing with the number of faces detected to catch proxies

VOLUNTEER & LEADERSHIP ACTIVITIES

1. **Executive Council Member and Treasurer of Institute of Electrical and Electronics Engineers (IEEE) Student Branch, IIT Ropar** *(Aug'17 - Aug'19)*
    - Organized lecture series by professors on advanced VLSI topics for first-year students and sophomores
    - Organized circuit design competitions
    - Conducted sessions on VLSI topics, interview questions, and EDA tools to prepare students for internship and job placements
    - Formed advising committee to help junior-year students connect with potential professors based on their research interests
2. **Robotics Club Head & Representative, IIT Ropar** *(Aug'17 - Aug'18)*
    - Handled club's electronics-related technical expertise
    - Managed a team of 8 club volunteers
    - Responsible for club's annual activities plan
    - Responsible for annual budget allocation for projects and contests
    - Supported members' nationwide participations in events and competitions
    - Organized training sessions on programming and working principles of microcontrollers (Arduino, Raspberry pi), sensors, actuators, etc.
3. Head coordinator for ROS workshop conducted under PunjRobotics, IIT Ropar
4. Member of Event Management Team of Advitiya'16, the Technical Festival of the Institute
5. Member of Sponsorship Team of Zietgiest'16, the Cultural Festival of the Institute
6. Mentored a group of 5 incoming students under the Institute Student Mentorship Program

ACADEMIC HONORS & ACHIEVEMENTS

1. Institute Merit-cum-Means (MCM) Scholarships for academic excellence in undergraduate study.

RELEVANT COURSES

EECS 413 Monolithic Amplifier Design (A+)
EECS 598 Advanced Analog and Mixed Signal Design
EECS 523 Digital Integrated Technology (A)
EECS 522 Analog IC Design